ECS5311-Advanced Digital Logic Notes

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1 Tuesday 8/27/2024

Definition 1 (Diode)**.** *Allows 1-direction current*

- .7V drop common due to silicon; the drop changes due to material.
- For semicondudctors to work, ned 4 bonds on the molecule.
- Made of 2 types of materials; P and N type materials.
  - Technically made of P-N junction.
  - 3 diodes in a transistor (NPN or PNP)
  - Determine if allow it to be controlled by current or field.
- look at schroedinger's wave equation
  - know wave is proportionate to energy
  - can get likelihood if we square the
  - begin with hydrogen, only 1/eletron so 1 interaction
- how do we determine electric force between 2 charge carriers?
  - force equation between two masses like gravity
  - see figure 1
- How do we go from force to energy? integrate over force equation: end up with $\frac{1}{r}$
  - see fig 2
  - How should we plot this? we need to figure r_1, r_2 for integral; picking different break poitns
  - 13.6 eV: lowest state in hydrogen atom, good poitn of reference
    - call this **ionizing break point**
  - -3.4 eV; next breaking point
  - 2 electrons can sit at the base state; every energy state can have up to 2
    - fairmions have spin 1-half; this allows an atom to hold two: one spins up, other spins down
    - boson's can have infinite at an energy level
  - If i add a third electron, this creates a *band*
    - The jump from 13.6 to 3.4 creates a band gap

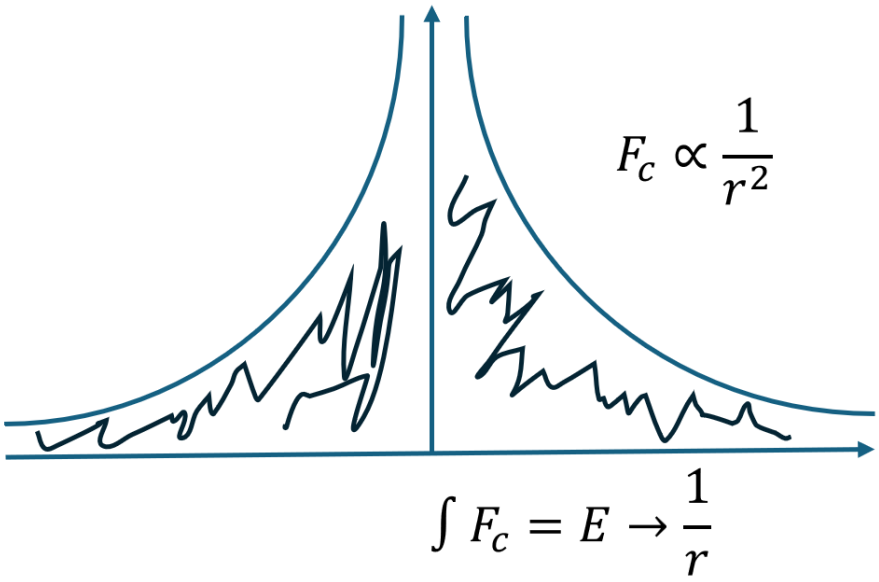

Figure 1: Force Plot

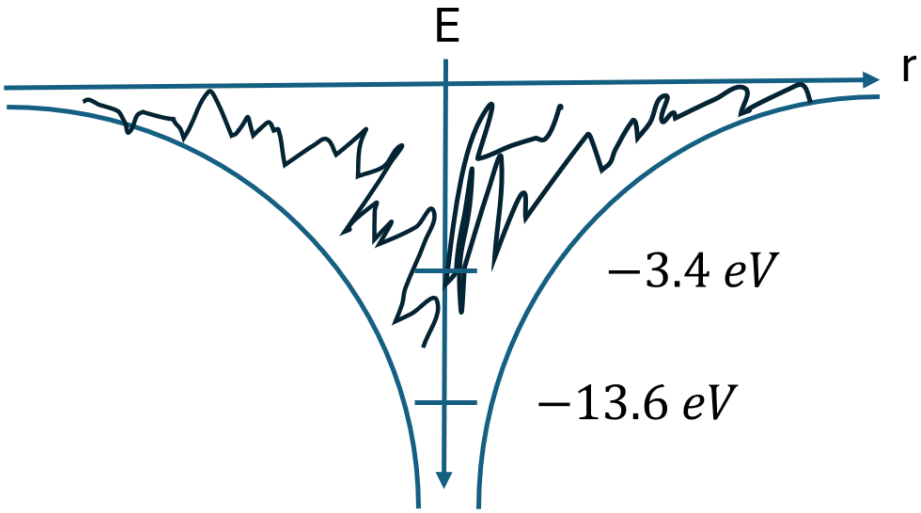

Figure 2: Energy Plot

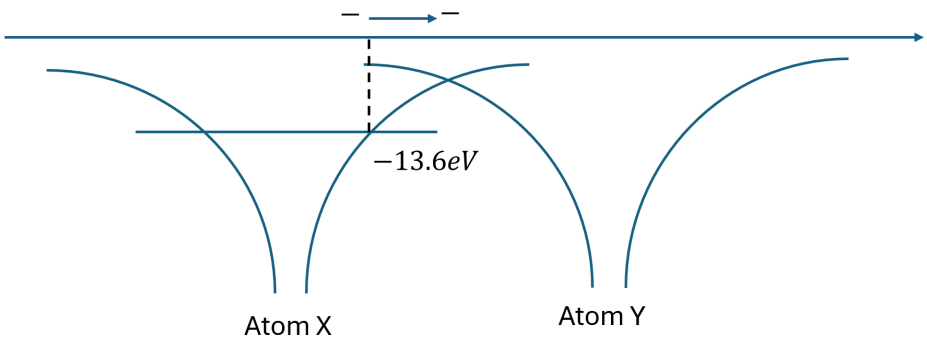

Figure 3: electron jump

* see fig 3
* Electron A, also has some elctron to atom B

    - at position 2, there's much less of an energy drop
    - if you move the two atoms together, the energy required to move is even lower
    - will result in bifurcation and split, thus spreading energy and keeping all 4 positions
    - by heisenberg uncertainty principle, don't know exact position and velocity; we know $\delta p - \delta x < \bar{h}$, nothign to do with how you observe, just that you observe
    - as atoms brought together, wave function from both added together
    - closer ot the center, get lower energy state; bands results from pauli exclusion and force when bringing atoms together
  - this is how we get a **valence band**; take lowest energy band available

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Definition 2 (Fermi energy)**.** *gives "probabilty to be in a conduction or valence band"*

- intrinsic semi conductors
  - column 4 of periodic table
  - gap between valence and conduction is small
  - 4

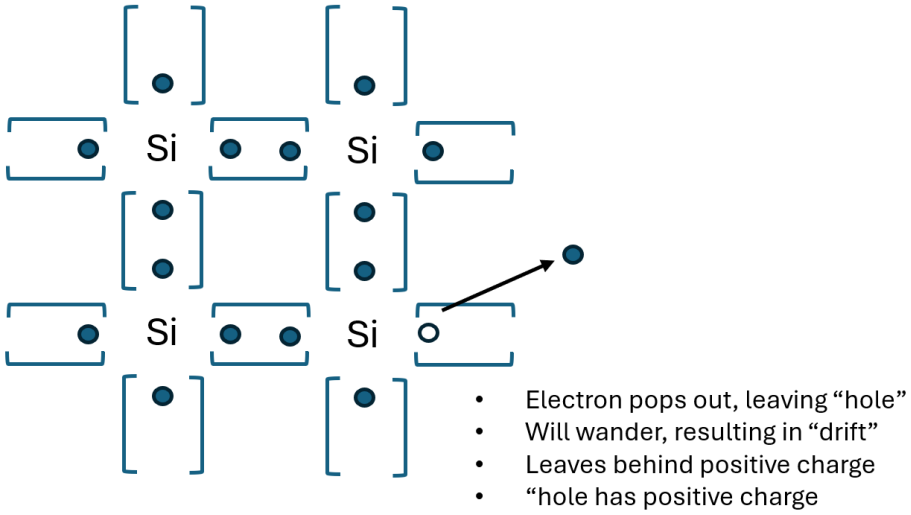

Figure 4: electron drift

  - Bonding drops to lower energy state
  - One electron in the bond will wnder off, leaving a hole
  - the hole and electron both considered carriers
  - if another electron pops off nad fils the hole, it iwl look like the hole moved
    - net effect is hole changing locations; hence holes also being carriers
    - how differences move slower than electrons move
  - P-type flow much slower than N-type due to difference in which carriers are *moving*
- We can boost number of carriers

- introduce new elements
- 5

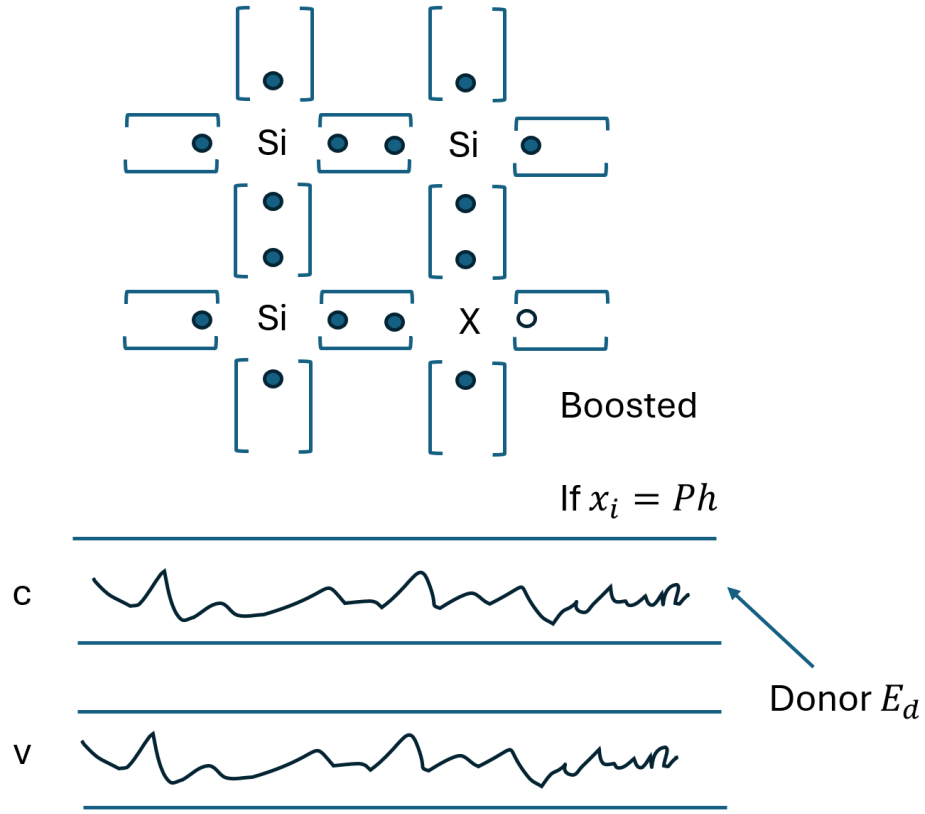

Figure 5: electron boost; ex Ph

- fermi energy moved up because energy needed for electron to move lowered significantly
  * now, energy to create holes also lower
- electrically neutral, even though electron is charge carrier
  * get majority carrier e^-
- we call this **extrinsic**; have doped with phosphorus (or any element that gives extra electrons)

- so why not add an element that introduces even more electrons?
  - more and more electrons begins adding elements that are nonmetlas
  - adding these elements result in more protons in addition to more electrons; more protons result in pulling down shell to a lower energy; now the energy needed ot jump between donor is even more
- Electron moving up/down the gap emits photons; this is how **LED**s work
- If we use boron (3 electrons on outer), only held together by 3 so less are held together; now hole is closer to top of valence band and Fermi energy also much lower. Will not have lower chance of hole moving; boron majority mover is a hole. Will need to be holes moving from borong to boron, looks like hole flowed to a silicon
- boron results in + holes as a majority carrier; phosphorus results in e^- electrons as majority carrier

- img3
- When P placed next to N, can move into P resulting in true net positive and net negatives in a region; this is called depletion region (depleted of charge carriers)
  - Depletion region fills really fast
  - This is called an insulator; this is a diode
  - There is a voltage differential due to this movement locally
- img5
- What happens if I connect P to N via battery?
  - will try to push electrons in one direction (holes in another)
  - will force electrons from P and N to jump call this **forward bias**
  - reduces depletion zone; with enough voltage from battery, depletion zone disappears and becomes a conductor
    - .7V or more
- img6
- Reverse bias
  - battery flipped; tries to force electrons. there will be some flow, but results in depletion region to increase
  - call this "avalanche region" (view graph, negative flow)
- img7
  - can B be negative V? no
  - can B be positive V? yes; is we hoook up voltage source at end
  - diode prevents output from being .3V (the minimum)
  - if we know .3V at B, what do we know?
- img8
  - If input is 0, just wants somethingto be $> -.7V$
  - need a pull-down resistor; allows Z to become 0
  - use ohm's law to determine resistor needed: $V = IR$
  - For 0,1, will pick $max(.7, 5.7)$ for the argeement region; .7 (in ii) results in 0
  - ii, introduce pullup resistor
  - this is diode logic; downside is voltage differential results in decreasing voltage

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- Review of last time, P/N results in a diode
- What if we add another N in front of P? get a new depletion zone
- img1
- with enough charge carriers through via forward bias, will remove the depletion zone and leak over and remove othe rdepletion zone; this results in essentially a wire

  - If I lower forward bias, less charges and flow eventually stops; similar to *variable resistance*, but not a resistance "on area here but over there", this is considered a trans-resistor or ***transistor***
  - can also be used for amplification, but we're only focused on using this a a ***switch***
  - there can also be electrical-mechanical switches (relay), but many advantages of an electrical switch
    * speed, lower power, more relliable, smaller, etc
- img2
- photo-resist layer $\rightarrow$ introduce light results in P/N wells with each iteration
  - all set in N type materical; prevent things from flowing. isolates N, prevents leakage
- will redraw since we only use left size; this is BJT
- another way to construct bjt: img3]

c	c	c
0	0	0
0	1	0
1	0	0
1	1	V-.7

  - logic: any diode with 1, essentially not there. Thus, $1|1$ results in resistor pull-up
- Note, output not very strong. Similar to diode logic, controlled by original sigl. Not as strong as original signla, but not limited to only one configuration.
- Have AND gate, but now we want to amplify
  - how to build an amplifier?
- img3
  - If A high (say $5V$), then B flows/turns on ($5 - .7 = 4.3V$ output). this will burn out, so need to stop current
    * easiest with a resistor
    * resistor on ground will result in raising the voltage, which we don't want because it changes output
    * Thus, we put resistor in beginning right after A inflow
    * Low resistance pulls down to 0 very hard; gives us a good zero
    * Resistor A for current limit
    * If nothing flowing through, ground/bottom connection is ignored, so output to B is whatever is hooked up to B
    * If we attach a pull-up resistor, won't affect pulldown
    * Strong outflow; this is an inverter amplifier
- img4
  - Now take our previous AND gate, combine it with inverter amplifier
  - know $D = AandB, C = NOT(D)$
  - Now have a NAND gate; a universal gate

    - aything can be written as sum of products; this is why NAND is considered universal, same as an NAND leading into another NAND
    - Same can be done with NOR gate
  - NAND build with NPN, NOR with PNP. NPN better, this is why NAND used more commonly than NOR. Slightly faster because we primarily use electrons vs holes

- With more and more gates, we get more current flowing in; let's say 16 input AND gate. One transisor allows lower latency, but also means more current coming in. Too much and can overload.

- img5
  - This is a totem pole
  - Want to either turn on bottom half and hoook to ground or turn on top and hook up to power

A	B	T_1	T_2	C
0	0	Off	Off	Z
0	1	Off	On	0
1	0	On	Off	$A - 1.4$
1	1	On	On	0 (I, high current)

- What if I had a middle zone? introduce resistor right after A and B, $R1$ and $R2$
  - For $D = 1$, get resistors AKA resistor divider $\frac{max(R_1,R_2)}{R_1+R_2}$
  - Now for $D = 0$, get $A = 1$, $B = 0$
  - We want $D = 1$ to be $A = 0$, $B = 0$; A needs to be bigger than both voltage drops (ie 1.4), so set $A < 1.4$, B greater than 1 drop ie $B > 0.7$
  - is it possible to satisfy both conditions? Yes. under this configuration, A cannot be above .7 so A and B can never be both on. Transistor 2 will cut voltage off form A
  - Transistors turn on really fast and give lots of power

- Why PNP good for power?
  - img6
    - Can only transfer $H - .7V$ vs the full H

4 Thursday, 9/5/2024

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Definition 3 (Bipolar Junction Transistor-BJT)**.** *Due to two junctions inside*

  - How to describe? with two diodes
  - how to control current, turn on/off? provide voltage to base which removes depletion region. We're applying current to remove region, which is why BJT's are alled *current control devices*
  - What happens whne you get voltage+current? Power aka heat. We don't like power use. This is hwy we don't like BJT's. Because they're current controlled devices, need decent amount of current power, so there is a minimum amount of power you can hit
  - dont like heat because:
    - will cause excitation

    - will induce mechanical failure
    - volume/heat will grow cubically, but the removal of heat is by a squared factor
  - want something that doesnt need so much current (so not a current controlled device), so instead will use a field-controlled device, leading to ***FET***'s

- Reduce current to reduce power
  - img1
  - If we introduce an insulator, we reduced current but no longer have a way to control the ates easily; how can we apply an electric field to remove the dead region?
    - capacitor
    - Add conductor on top of insulator
    - Will briefly get flow. Insulator will get excited
    - The $5V$ pulls electrons in. If they're flowing up, the plate gets positively charged. The Insulator then becomes negatively charged, but the insulator prevents charges from moving so it builds up and created a tiny layer of N-type; built a wire
    - N all the way across so it will flow great; took very little current, hence this is a field effect (and not resulting from current)
    - Depletion not removed, simply building conductor where we want it
    - thus, power lower due to lower current

- So how can I build the insulator layer?
  - Thin oxide layer? Silicon dioxide layer, titanium dioxide layer
  - Can oxide just in one area build to a ***metal oxide semiconductor (MOS)***

- Same can be done for a PNP
  - img2
  - Instead, connect to ground; positive/negative sides switched

- BJT can be faster

- **Definition 4** (Metal Oxide Semiconductor-NMOS)**.** *NPN*
  - power is "on", ground is "off"
  - better at switching ground (similar to how NPN is)

- **Definition 5** (PMOS)**.** *a PNP*
  - negatives on top allow it to work, hence the dot on top of hte circuit symbol
  - Ground is "on", power is "off"
  - better at swithing power (similar to how PNP is)

- Ideally want to build circuit that supplies 1's and 0's (because NMOS/PMOS better with power and ground)
  - So we want things flowing into gate; charge or discharge gate

  - Just like BJTs, to use base, need to hook power or ground. We used pullup resistors then eventually built totem pole. For MOS, we're goign to first build something using transistors
    * Power network above will supply all 1's, ground network above will supply all 0's
  - img3; statis CMOS logic
  - Don't want both on at once; will result in a short (no resistor so power iwll go to ground); we don't want a resistor to not be slowed down
  - Also don't want both off
    * Build with Karno Map (kmap)

- img4
  - Step 1, what's the power?
    * Power on PMOS, so power only flows when both on, so this is an AND of some case due to series of two
    * draw kmap
      · topleft is power network; where is ground netowrk?
      · dont want Z's, don't want short, so where do zeros go? everywhere else
      · powers of two, have to be aligend horizontally (h1) and vertically (v1)
      · So what is the vertical 0's? How do we hook up NMOS to get a 0 when A is 0? Connect NMOS to A, B separately
    * This is a NOR gate

- img5
  - Now let's build a NAND gate
    * PMOS since if B or A is 0, we want to supply power; connect A, B to PMOS
    * Independent so can onnect to power separately
    * Need both A and B on, so need to be connected in series to be connected to ground

- img6
  - Notice the flip/complement between A/B/C in the PMOS and CMOS being in parallel and series

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- Static CMOS: called static because the signal stays the same/ stays valid across all time
  - Slow; pullup/pulldown operate at different speeds
    * down significantly faster due to NMOS being used for pulldown network; primary charge mover is the electrons
    * note: voltage is related to time, so want lower voltage
    * Charge carriers are slow when dealing with holes, so need more charge carriersm but to get more, need ot make it "bigger" but making it bigger leads to higher capacitance (C)
    * In general, to make it more reaosnable, capacitor needs to be bigger for PMOS gates; approximately 3x bigger; unfortunately, bigger capacitor results in taking more time to turn on (ie full state), so not much you can do to make it faster
      · ***Good for transferring power, but big nad slow***